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# Data Sheet

## Simulated 20 nm Embedded Processor Core Sample Test Case
## e.g. ARM Processor

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This is a preliminary version of a small processor core, similar to an ARM processor. It is 487.2 microns wide and 422.4 microns high.

The design files are in a TAR archive called "demo_small_cpu_2013Mar15.tgz", which is about 95.8 megabytes in size. On a Linux/Unix system, unpack it using the command "tar xzf demo_small_cpu_2013Mar15.tgz". The full GDSII file is about 637.6 megabytes in size and the full OASIS file is about 38.3 megabytes in size.

This demonstration design file is meant to show the cell generation, placement and routing, and floorplanning capabilities of the Yotta Data Sciences synthetic design/stress test case generator. The processor core in it is part of Yotta's IP library; it is placed 26 times in the fourth stress test case (the network processing SoC).

The processor core includes 16 kilobytes of level 1 cache SRAM; there are also small memory blocks for register files. Altogether there are 305,536 bits of SRAM including ECC. After expanding all design hierarchy, there are 208,590 placed standard cell instances and 3,742,260 transistors.

Like all of the initial designs in the stress test suite, this processor core uses 20 nm design rules. Transistor gates are 20 nm long; the gate layer routing pitch is 72 nm. Metal layers can be routed using a pitch as small as 64 nm, as is done in SRAM blocks. Standard cell routing uses the gate layer routing pitch of 72 nm.

The GDSII and OASIS layer definitions are as follows:

```
N well       layer 2, datatype 0
N diffusion  layer 4, datatype 0
N substrate  layer 5, datatype 0  substrate tiedowns
P diffusion  layer 6, datatype 0
P substrate  layer 7, datatype 0  N-well tiedowns
Gate         layer 9, datatypes 0 and 1; 20 nm width, 40 nm spacing,
             72 nm pitch with contacts
N+ implant   layer 11, datatype 0
P+ implant   layer 13, datatype 0
Contact      layer 17, datatypes 0 and 1; 32 nm width, 32 nm spacing
Metal 1      layer 18, datatypes 0 and 1; 32 nm width, 32 nm spacing
Via 1        layer 19, datatypes 0 and 1; 32 nm width, 32 nm spacing
Metal 2      layer 20, datatypes 0 and 1; 32 nm width, 32 nm spacing
Via 2        layer 21, datatypes 0 and 1; 32 nm width, 32 nm spacing
Metal 3      layer 22, datatypes 0 and 1; 32 nm width, 32 nm spacing
Via 3        layer 23, datatypes 0 and 1; 32 nm width, 32 nm spacing
```

```
Metal 4      layer 24, datatypes 0 and 1; 32 nm width, 32 nm spacing
Via 4        layer 25, datatypes 0 and 1; 32 nm width, 32 nm spacing
Metal 5      layer 26, datatypes 0 and 1; 32 nm width, 32 nm spacing
```

Polygons for gate, contact, and metal layers are colored for double patterning using datatypes 0 and 1.

Data on the gate and metal layers includes port rectangles with datatype 2. These can be ignored.

The tar archive includes three files:

demo_small_cpu_2013Mar15.gds
demo_small_cpu_2013Mar15.oas
demo_small_cpu_floorplan_2013Mar15.gds

The floorplan GDSII file represents the design hierarchy and block boundaries without any transistors or routing, so it is very small (6 kilobytes). Each cell in the floorplan file represents a placed block in the design, allowing a quick understanding of the organization of the design.

Note that the design files contain a preliminary version of the processor core, which does not yet include inter-block routing (metal 6 and up), metal fill, or pad rings.